MP1010B
Cold Cathode Fluorescent Lamp Driver

The Future of Analog IC Technology

DESCRIPTION

The MP1010B is a power solution IC that offers a true complete solution for driving a Cold Cathode Fluorescent Lamps (CCFL). This Power IC converts unregulated DC voltage to a nearly pure sine wave required to ignite and operate the CCFL. Based on proprietary power topology and control techniques it greatly increases the power conversion efficiency.

EVALUATION BOARD REFERENCE

Board Number	Dimensions
EV1010B-00A	3.75"X x 0.4"Y x 0.25"Z

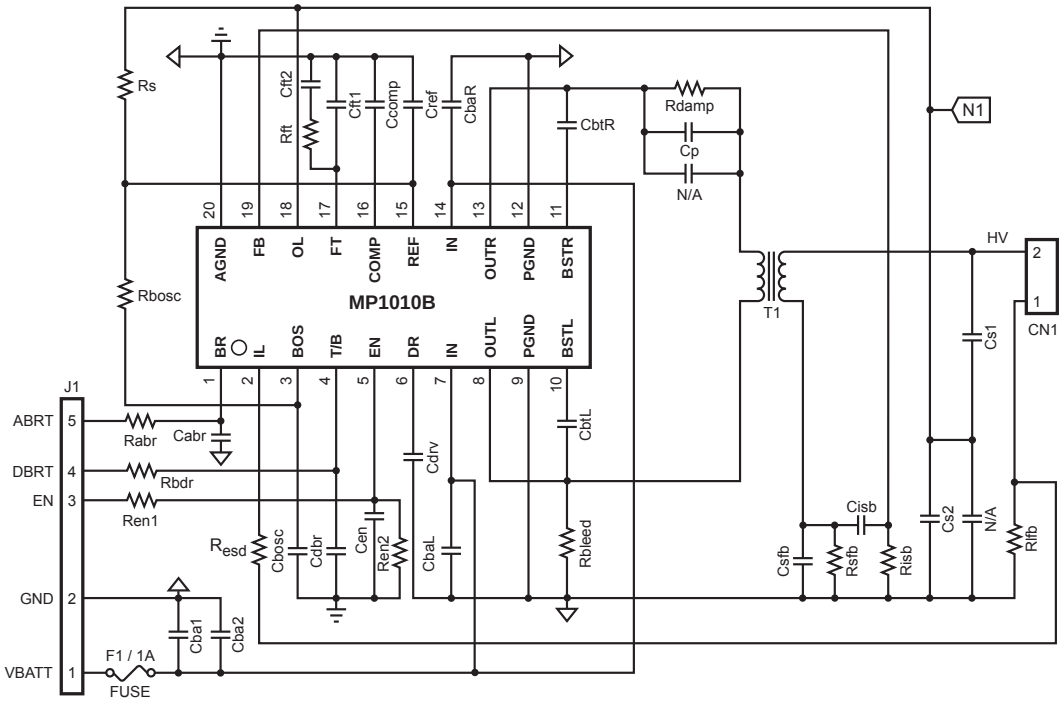
FEATURES

- Integrated Power Switches
- 6.0V to 23V Variable Supply Voltage with Regulated Lamp Current.
- Rated 12W Power Output at 12V Input
- Open Lamp Regulation
- Current and Voltage Feedback Control
- Logic Level Burst Mode Control
- Supports Open/Short Lamp Protection
- Soft-Start
- Short Circuit Protected Output
- High Energy Start Pulse
- Analog and Burst Mode Dimming

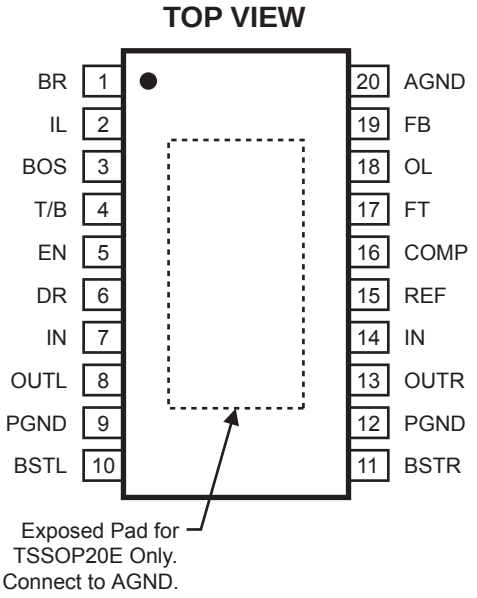
APPLICATIONS

- LCD Backlight Inverter for Notebook Computers
- Web Pads, GPS, Desktop Displays, Portable DVD, Car Video Display Systems

TYPICAL APPLICATION



PACKAGE REFERENCE



Part Number*	Package	Temperature
MP1010BEM	TSSOP20	–20°C to +85°C
MP1010BEF	TSSOP20E	–20°C to +85°C

* For Tape & Reel, add suffix –Z (eg. MP1010BEM–Z)
For RoHS Compliant Packaging, add suffix –LF
(eg. MP1010BEM–LF–Z)

ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage (V_{IN}) 25V
IL, FB Input Voltages (V_{IL}, V_{FB}) .....±6V
OL Input Voltage (V_{OL}) ..... –0.3V to +12V
Logic Input Voltages ..... –0.3V to +6.8V
Power Dissipation 1.0W
Operating Frequency 150KHz
Junction Temperature ..... 150°C
Lead Temperature (Solder) ..... 260°C
Storage Temperature ..... –55°C to +150°C

Recommended Operating Conditions (2)

Input Voltage (V_{IN}) ..... 6V to 23V
Analog Brightness Voltage (V_{BR}) ..... 0V to 1.9V
Digital Brightness Voltage ($V_{T/B}$) ..... 0V to 1.8V
Enable (V_{EN}) ..... 0V to 5V
Operating Frequency (Typical) 60KHz
Ambient Operating Temp ..... –20°C to +85°C

Thermal Resistance (3)

	θ_{JA}	θ_{JC}	
TSSOP20	90°	25°	C/W
TSSOP20E	40°	6°	C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Reference Voltage						
Output Voltage	V_{REF}	I_{REF} = 3mA	4.75	5.0	5.25	V
Reference Current	I_{REF}				3.0	mA
Line Regulation		6.5V < V_{IN} < 23V			30	mV
Load Regulation		0mA < I_{REF} < 3.0mA			30	mV
Output Drivers						
Switch On Resistance (4)	$R_{(ON)}$		0.08	0.11	0.14	Ω
Short Circuit Current	I_{SC}			4		A
Minimum On Time	$T_{ON(MIN)}$	V_{COMP} = 0V, V_{IN} = 23V		435	550	ns
Minimum On Time	$T_{ON(MIN)}$	V_{COMP} = 0V, V_{IN} = 6V		1750	2100	ns
Battery Supply						
Supply Current (Quiescent)	$I_{CC(OFF)}$				10	µA
Supply Current (Operating)	$I_{CC(ON)}$	V_{IN} = 23V		1.8	2.5	mA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Brightness Control						
Sense Full Brightness	V_{IL_MAX}	V_{BR} = 2.0V	360	379	400	mV
Sense Full Dim	V_{IL_MIN}	V_{BR} = 0V	105	117	130	mV
Lamp Current Regulation		7V < V_{IN} < 23V		2	5	%
Burst Oscillator Peak Voltage	V_{BOS}		1.70	1.78	1.86	V
Digital Brightness Offset Voltage	$V_{(OS)\ T/B}$		-50	5	50	mV
Fault Detect						
Open Lamp Threshold	$V_{(TH)OL}$			0		V
Secondary Current Threshold	$V_{(TH)FB}$		1.1	1.2	1.3	V
Fault Mode COMP Current	I_{COMP}	V_{OL} < 0V, V_{FB} > 1.2V		475		µA
Shutdown Logic						
Fault Timer Threshold	$V_{(TH)FT}$		1.1	1.2	1.3	V
Fault Timer Sink Current		V_{OL} > 0, V_{FB} < 1.2V		1		µA
Fault Timer Source Current						
Open Lamp		V_{OL} < 0, V_{FB} < 1.2V	0.5	1	1.5	µA
Secondary Overload		V_{FB} > 1.2V	90	120	160	µA
Enable Voltage Low	$V_{(L)EN}$				0.5	V
Enable Voltage High	$V_{(H)EN}$		2.0			V

Note:

4) This parameter is guaranteed by design.

PIN FUNCTIONS

Pin #	Name	Description
1	BR	Analog Dimming.
2	IL	Lamp Current Feedback Sense Input.
3	BOS	Burst Oscillator Timing.
4	T/B	Test/Burst Mode Dimming.
5	EN	Chip Enable. ***Do not float this pin.***
6	DR	Internally Generated MOSFET Gate Drive Supply Voltage (6V).
7	IN	Power Supply Input.
8	OUTL	Output to Load (Tank Circuit).
9	PGND	Power Ground.
10	BSTL	Regulated Output Voltage for Bootstrap Capacitor on Phase L.
11	BSTR	Regulated Output Voltage for Bootstrap Capacitor on Phase R.
12	PGND	Power Ground.
13	OUTR	Output to Load (Tank Circuit).
14	IN	Power Supply Input.
15	REF	Internally Generated Reference Voltage Output (5V).
16	COMP	Loop Compensation Capacitor.
17	FT	Fault Timer.
18	OL	Open Lamp Detect (Lamp Voltage Feedback).
19	FB	Shorted Lamp Detect (Secondary Current Feedback).
20	AGND	Small Signal Ground (5).

Note:

5) For the MP1010BEF, connect the exposed paddle to AGND (Pin 20).

BLOCK DIAGRAM

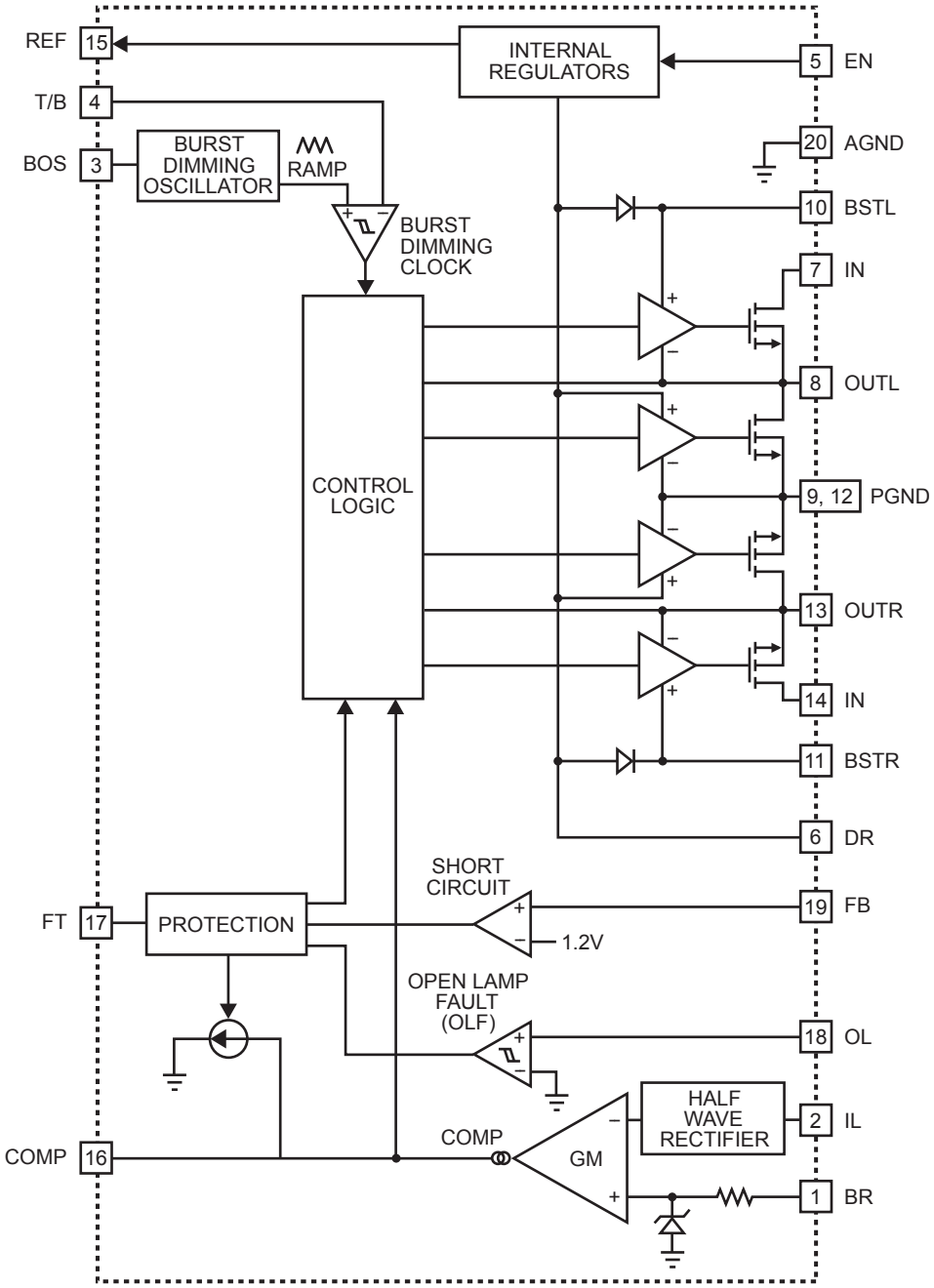


Figure 1—Functional Block Diagram

APPLICATION INFORMATION

Brightness Control

The maximum lamp current is set by Rlfb:

$$Rlfb = \frac{2.2 \times V_{IL\_MAX}}{I_{LAMP\_RMS}}$$

Where V_{IL_MAX} = 379mV, typically. For a 6mA$_{RMS}$ lamp current, Rlfb = 139Ω. Use a 140Ω ±1% resistor for the application.

The MP1010B can adjust the lamp brightness in three operating modes: Analog Mode, Burst Mode with a DC input, or Burst Mode with external PWM. The Burst Mode with a DC input is not recommended if the dimming steps required are more than 10. For such applications, please select the MP1016 or MP1028.

The three modes are dependent on the pin connections as per the table below.

Table 1—Dimming Mode Selection

Options	Pin 1 (ABRT)	Pin 4 (DBRT)	Pin 3 (BOSC)	
			Rbosc	Cbosc
Burst Mode with PWM Input	V_{REF}	PWM	220kΩ	100kΩ
Analog Mode with DC Input	0V to 1.9V	V_{REF}	220kΩ	100kΩ/ 47nF
Burst Mode with DC Input	V_{REF}	0V to 1.8V	220kΩ	47nF

The PWM signal should be 200Hz (±50Hz) for the best possible performance. For different panels, the burst frequency may need adjusting to avoid possible interference with the LCD horizontal scan frequency. The PWM signal High level should be larger than 1.7V but less than 5V. The Low level should be smaller than 0.7V but higher than 0V. It is recommended that the PWM minimum pulse be longer than 250μs, and that the pulse rising and falling edges be less than 0.5μs. The PWM signal should be connected to the DBRT pin directly (Rdbr = 0Ω and remove Cdbr).

For an application with either Analog Mode or no dimming, the BOSC pin can be shorted to Analog GND to simplify the circuit.

For analog dimming, a voltage between 1.9V and 5V sets the maximum brightness. 0V sets the minimal brightness, wherein lamp current is 1/3 of the maximum value. Most applications need a RC filter to eradicate noises before the DC signal reaches the ABRT pin. The suggested values are Rabr=47kΩ, Cabr=0.1μF.

For burst dimming with a DC input, a voltage between 1.8V and 5V sets the maximum duty cycle (100%). 0V sets the minimum duty cycle, which is related to the design of Rbosc and Cbosc. Again, most applications need a RC filter to eradicate noises before the DC signal reaches the DBRT pin. The suggested values are Rdbr=47kΩ, Cdbr=0.1μF.

Select Rbosc and Cbosc based on the following:

1. Select a burst frequency f_{BOSC} for the panel.

2. Design the minimal duty cycle to meet the minimal pulse request for the lamp.

$$D_{MIN} \geq 250\mu s \times f_{BOSC}$$

3. Determine Rbosc by the formula:

$$Rbosc \cong \frac{1.68}{0.42 \times D_{MIN} \times 350 \times 10^{-6}}$$

4. Determine Cbosc by the formula:

$$Cbosc \approx \frac{(1 - D_{MIN})}{0.42 \times Rbosc \times f_{BOSC}}$$

For a typical design, Rbosc=220kΩ and C1=47nF.

Fault Protection

Open Lamp: The OL Pin (#18) is used to detect whether an open lamp condition has occurred. A capacitor divider (Cs1 and Cs2) is used to feedback the lamp voltage to OL with a DC bias of V_{REF} through Rs. During normal operation the OL pin is typically at 5V DC with an AC swing of less than 4V in amplitude. If an open lamp condition exists, the AC voltage on the OL line will swing below zero volts. When that occurs, the IC regulates the OL voltage to 10V p-p and a 1μA current source will inject into the FT pin. If the voltage at the FT pin exceeds 1.2V, then the chip will shut down.

Accordingly, the open lamp voltage can be set using the capacitor divider.

Cs1 must be rated at 3KV or above. Its value is typically between 10pF to 22pF.

$$Cs2 = \frac{Cs1 \times V_{STRIKE\_MAX}}{3.5V}$$

Where V_{STRIKE_MAX} is the required maximum lamp striking voltage in RMS value.

The value of Rs is typically 100kΩ. It is not critical as long as the resistance is much larger than the impedance of Cs2.

Excessive Secondary Current (Shorted Lamp and UL safety specs): The FB pin (#19) is used to detect whether excessive secondary current has occurred. During normal operation the peak FB voltage is below 1.2V. If a fault condition occurs that increases the secondary current, then the voltage at FB will be greater than 1.2V. When that occurs, a 120μA current source will inject into the FT pin. If the voltage at the FT pin exceeds 1.2V, then the chip will shut down.

The following is the design reference for the secondary winding current.

Sensing network: Rsfb, Risb, Csfb and Cisb.

$$Rsfb > \frac{1.2V}{0.7mA} = 1.7k\Omega$$

The recommended value is 3.9kΩ to 10kΩ (typically 4.7kΩ).

$$Csfb < \frac{0.7\,mA/KHz}{1.2V \times 2\pi} = 93nF$$

Select a capacitor with less than 93nF capacitance for Csfb and make the FB pin voltage peak value around 0.7V in normal operation.

The 0.7mA DC and 0.7mA/KHz AC current values are taken from the UL60950 safety requirement.

Cisb and Risb make up a high-pass filter, wherein the corner frequency should be between 1KHz and 2KHz so as to minimize the attenuation of the AC signal.

The recommended value for Risb is 100kΩ.

$$1.6nF = \frac{1}{2\pi \times Risb \times 1KHz} > Cisb$$

$$Cisb > \frac{1}{2\pi \times Risb \times 2KHz} = 0.8nF$$

A typical value for Cisb is 1.2nF.

Fault Timer: The timing for the fault timer will depend on the sourcing current, as described above, and the capacitor on the FT pin. The user can program the time for the voltage to rise before the chip detects a “real” fault. When a fault is triggered, then the internal drive voltage (V_{Dr}) will collapse to 0V.

Rft, Cft2 and Cft1 form the fault timer circuit. The recommended value for Rft is 100kΩ.

For open lamp time:

$$T(open\_lamp) = \frac{Cft2(\mu F) \times 1.2V}{1\mu A}$$

For secondary short turn off time:

$$T(short) = \frac{Cft1(\mu F) \times 1.2V}{120\mu A}$$

A typical value for Cft2 is 1μF. Cft1 should be much smaller than Cft2, which makes the short circuit protection speed very fast. The recommended value for Cft1 is between 1nF and 10nF.

If the protection speed for the secondary short is not critical, the fault timer circuit can be simplified as a single 1μF capacitor connected to the FT pin.

Lamp Startup

The strike voltage of the lamp will always be guaranteed at any temperature because the MP1010B uses a resonant topology for switching the outputs. The device will continue to switch at the resonant frequency of the tank until the strike voltage is achieved. This eliminates the need for external ramp timing circuits to ensure startup.

Chip Enable

The chip has an on/off function, which is controlled by the En pin (pin #5, cannot be left floating). The enable signal goes directly to a Schmitt trigger. The chip will turn ON when En is High (>2V) and OFF when it is Low (<0.5V). It is recommended that power be applied to the MP1010B via the IN pins (#7 and #14) a minimum of 3ms prior to the En pin (#5) being switched high.

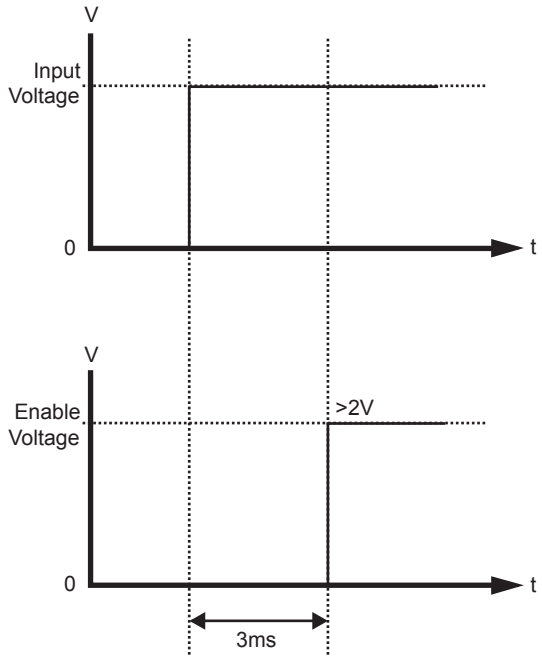


Figure 2—Input Voltage vs. Enable Sequence

Design Guidelines

Ccomp is the system compensation capacitor that connects COMP and AGND. A 1.5nF or 2.2nF X7R ceramic cap is recommended. Its value affects the lamp current soft-on rising time and soft-off falling time in burst mode. This capacitor must be placed as close as possible to the related pin.

Cref is the bypass capacitor for the internal 5V supply. Cdrv is the bypass cap for the 6.2V gate drive supply. Cref and Cdrv should be 0.1µF, X7R (≥16V) ceramic capacitors. These capacitors must be placed as close as possible to the related pin.

CbaL and CbaR are bypass capacitors for the inverter input power. These capacitors will absorb most of the input switching current of the inverter and will require adequate current ripple rating. The typical current rating for these caps is >500mA$_{RMS}$. The typical value is 1µF to 2.2µF, X7R (≥25V) ceramic with low ESR value. These capacitors must be placed as close as possible to the related pin and with wide copper traces for the connection.

Cba1 and Cba2 are also bypass capacitors for the inverter input power. Their major role is for input filtering. The typical value is 2.2µF to 4.7µF. X5R or Y5U (≥25V) ceramic capacitors can be used.

CbtR and CbtL are bootstrap capacitors for the upper switches' gate drive. 10nF, X7R (≥16V) ceramic capacitors are recommended. These capacitors must be placed as close as possible to the related pin.

Cp is the DC blocking cap in the transformer primary side. It conducts large winding current (typically 0.8A$_{RMS}$), so low ESR X7R/X5R ceramic is required. The capacitance value is typically 0.47µF to 2.2µF. The voltage rating needs to be 16V or higher. It is better to use two parallel caps for minimal ESR losses.

The OUTL and OUTR pins are the bridge outputs, which conduct typically 0.8A$_{RMS}$ current. Wide copper traces should be used for the connections from IC pins to the transformer. In addition, the connection loop should be minimized to avoid the high dv/dt impact to other circuits.

Rdamp and Rbleed are used to ensure that the bridge outputs are 0V prior to startup. Typically Rbleed=4.3kΩ and Rdamp=1kΩ.

Resd is highly recommended to minimize the possibility of ESD damage in case of mishandling of the IC during board level assembly and test. A typical value is 1kΩ.

For most transformers, one terminal connection of the secondary winding is on the side of the primary winding. This side must be connected to the lamp cold side since it cannot handle high voltages.

The transformer secondary winding leakage inductance L_{LK2} is typically 250mH to 350mH (measured with primary winding shorted). The turns ratio is roughly:

$$n \geq \frac{V_{LAMP\_RMS}}{V_{IN\_MIN}} \times 1.1$$

Where V_{LAMP} is the lamp voltage in normal operation conditions and V_{IN_MIN} is the minimum input voltage for the inverter.

The open lamp resonant frequency is:

$$f_{OPEN} = \frac{1}{2\pi \times \sqrt{L_{LK2} \times Cs1}}$$

It is recommended that the resonant tank (transformer and Cs1) be designed so that f_{OPEN} is less than 100KHz. This is to avoid possible transformer arcing during open lamp conditions.

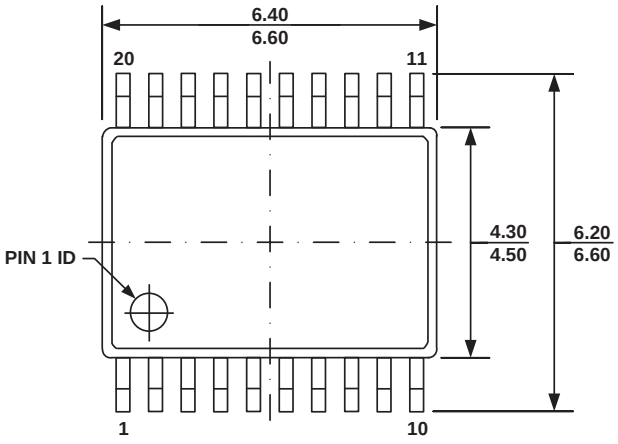
For better thermal performance, please use MP1010BEF (with exposed pad). Normally, there will be a large copper area for ground in the bottom PCB layer which can be used for heat dissipation. Connect the paddle to this ground. Many vias are needed in order to reduce the thermal impedance from the paddle to the bottom ground.

For the ground layout, it is better that the analog ground be connect with the power ground at a single point, at the AGND pin or the exposed pad. If the power ground in the bottom layer has sufficient surface area, this connection will not be as critical.

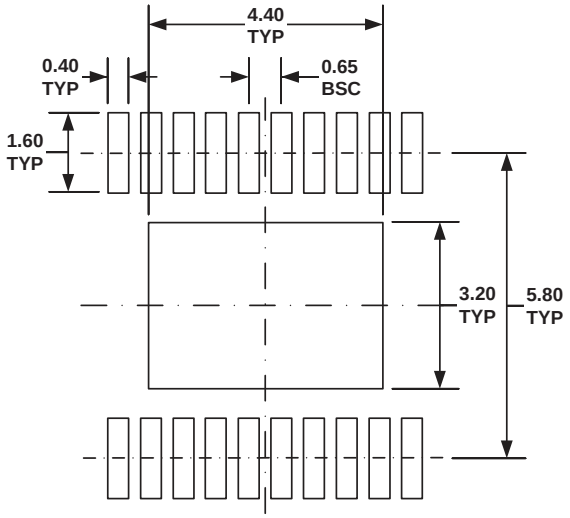
Please contact MPS for assistance with the resonant tank design if needed.

PACKAGE INFORMATION

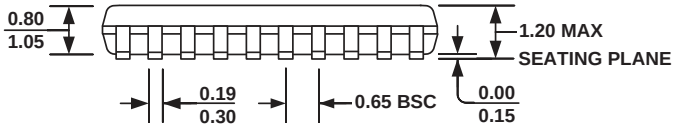
TSSOP20 OR TSSOP20E (EXPOSED PAD)



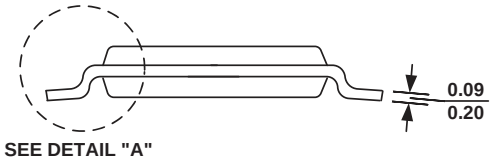
TOP VIEW



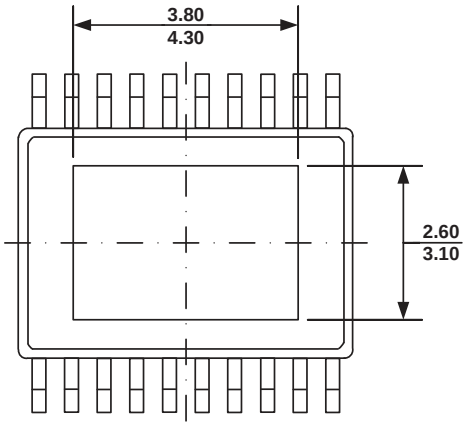
RECOMMENDED LAND PATTERN



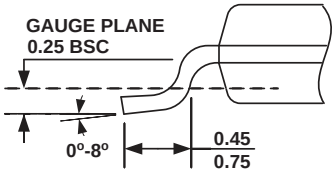
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL A

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ACT.
6) DRAWING IS NOT TO SCALE.

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